

## I/O CONTROLLER

### FEATURES

- **HT-1100 I/O Controller:**
  - HyperTransport™ Bus
  - PCI Express® 1.1
  - PCI 2.3 bus (32-bit 33 MHz)
  - USB 2.0 with debug port support
  - IDE
  - SAS/SATA
  - LPC (TPM 1.2-compliant)
  - SPI
  - SMBus (two masters at 400 KHz)
  - UAA HD audio
  - 16550-compatible UART
  - Legacy-free operation with 8042 register support
  - Watchdog timer
  - ACPI 3.0a-compliant
- **HyperTransport**
  - 8x link up to 2 Gbps (1 GHz)
  - Revision 2.0-compliant
  - CRC error generation and checking
- **PCI Express 1.1**
  - Eight lanes support, operating at 2.5 GHz
  - Two root complexes (masters)
- **USB 2.0**
  - 12 USB ports (three EHCI controllers)
  - MSI capability
  - Support for legacy USB keyboard and mouse
  - Support for legacy USB 1.1/2.0 operation
  - Support for one debug port controller
- **IDE**
  - Single-channel parallel ATA controller
  - Support for master and slave devices
  - ATA/ATAPI7 (UDMA133)-compliant
- **SATA/SAS**
  - Supports four devices
  - NCQ and staggered spin-up support
  - 3-Gbps SATA/SAS performance
  - MSI capability
  - SAS-compliant with SAS 1.1
- **SPI**
  - Support for system ROM (pin strap between SPI/LPC)
  - 40-MHz operation with support for two devices
- **ACPI**
  - Compliant to specification revision 3.0a
  - Power button support
  - S1, S2, basic S3, S4, S5 support

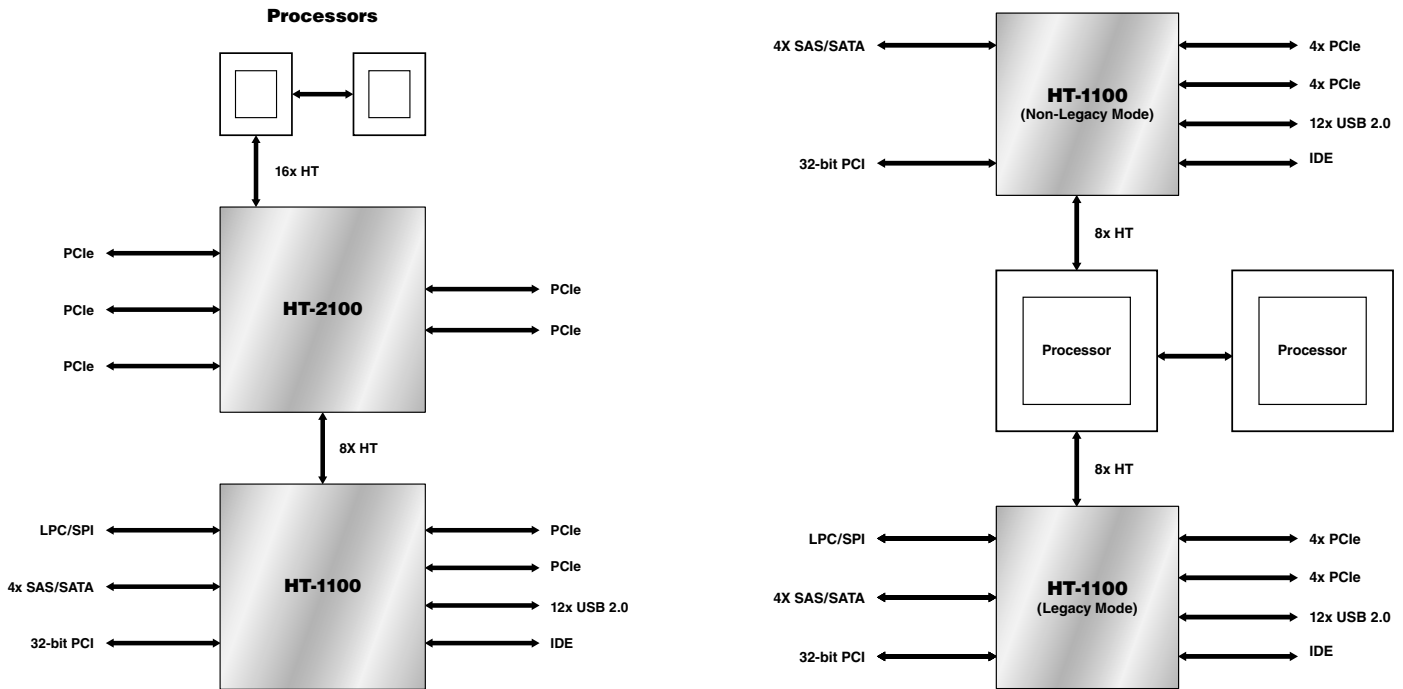
### SUMMARY OF BENEFITS

- **Multiprocessing SystemI/O controller for HyperTransport-enabled processors**
- **Performance, reliability, availability, scalability, and modularity**
- **Integration (PCI Express®, SAS/SATA, PCI, and USB 2.0—all in one chip)**
- **Best-in-class 64-bit performance**
  - HyperTransport-based architecture reduces I/O bottlenecks and improves overall system performance
  - Integrated processor memory controller minimizes latency, yielding better application performance
  - Best-in-class 64-bit and 32-bit performances
- **Industry-proven reliability and availability**
  - Reusable design methodology used with industry-proven functional blocks
  - Designed for 24/7 enterprise computing uptime
  - Advanced error detection and correction
- **Extensive scalability**
  - HT multiprocessor architecture allows superior per-processor scalability compared to similar x86 architectures
  - Individual HT link widths and clock speeds easily suit cost/performance targets
  - Multiple HT-1100/HT-2100 SystemI/O controllers deliver numerous I/O devices and slots
- **Modular architecture**
  - Modular building blocks allow platform designs that scale from the low end all the way to high end
  - SystemI/O modularity keeps costs low without sacrificing functionality
  - Modular design allows more freedom to differentiate from competition and is compatible with previous SystemI/O controllers (HT-2000, HT-1000, HT-2100)
- **The HT-1100 utilizes HyperTransport to interconnect to the CPU/host bridge and I/O bridge solutions. This building block approach enables OEMs to tailor a system to their applications.**

### TARGET APPLICATIONS

- **Unisocket to multisocket tower/rack/blade servers**
- **Workstation platforms**
- **Storage platforms (NAS, SAN, blades)**
- **Embedded designs**

# OVERVIEW



## Dual-Socket Multiprocessing Server Configuration

The HT-1100 is targeted at the volume server/blade and workstation market with the capability to efficiently span from 1–8 socket CPUs without incurring large latencies.

The HT-1100 is a highly scalable SystemI/O solution for 64-bit/32-bit processors that can be configured to meet the OEM's needs for a variety of product segments. The dual-socket configuration shown at the top of the graphic uses the HT-2100 as a tunnel to the processors. By combining the HT-1100 with the HT-2100, servers can support up to seven PCI Express Gen1 masters for a total of 32 PCI Express links. However, the HT-1100 can be used to connect directly to the processors, as shown in the upper right graphic, allowing a lower latency path to the processors and memory.

The 8x HT port can operate at up to 1-GHz double data rate in both transmit and receive directions to aggregate up to a total bandwidth of 4 Gbps. It is also backward-compatible to slower HyperTransport speeds.

For the next-generation low-latency, high-bandwidth I/O interconnect PCI Express, the HT-1100 offers eight lanes of PCIe™ Gen1 operating at 2.5 Gbps. With two PCIe masters, this can be used as one x8 lane, two x4 lanes, two x2 lanes, or two x1 lanes.

The SAS/SATA interface supports four ports, each of which can operate independently in either SATA or SAS mode and can transfer up to 3 Gbps.

Additional highlights include:

- NCQ support
- SAS 1.1-compliant
- SAS disk and tape support
- OS boot support
- MSI support

The 12 USB ports are compliant with Universal Serial Bus Specification 2.0, Open Host Controller Interface for USB Rev. 1.0a, and Enhanced Host Controller Interface for USB Rev. 0.95. All ports support legacy USB and MSI. In addition, one of the ports can be used as a debug port.

Other important features include integrated I/O APIC with 48 interrupts (32 are PCI), SMBus 2.0 specification-compliant interface, LPC-compliant to TPM 1.2, SPI supporting up to two devices, single-channel ATA/ATAPI6-compliant IDE, ACPI 3.0a-compliant, and UAA high-definition audio interface.

Additionally, previous generation SystemI/O controllers (HT-2000/HT-1000) can be used in conjunction with the common HyperTransport interface.

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